WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor package comprising:

forming a plurality of patterns formed plates, wherein each pattern formed plate is formed by:

forming first plated copper layers on upper and lower surfaces of an insulation substrate;

forming a pattern in the first plated copper layers formed at upper and lower surfaces of the insulation substrate; and

forming an opening by removing a central portion of the insulation substrate with the first plated copper pattern formed thereon;

forming a bonding pad pattern around the opening of at least one of the pattern formed plates, and forming a first coating layer with a non-copper metal material on the bonding pad pattern;

forming a laminated body by laminating the plurality of pattern formed plates to each other;

forming a second plated copper layer by forming a through bore in the laminated body and forming a second copper plating on the through bore and the first coating layer; and

forming a bonding pad by removing the second plated copper layer formed on the first coating layer, and forming a second coating layer with a non-copper metal material on the first coating layer.

2. The method of claim 1, wherein the insulation substrate is formed of one of glass epoxy, glass polyimide and a bismaleimide triazine resin.

3. The method of claim 1, wherein forming the plurality of pattern formed plates comprise forming openings in each of the plurality of patterns formed plate, wherein each of the openings are formed with different sizes.

4. The method of claim 1, wherein the first coating layer is a nickel/gold plating layer.

5. The method of claim 4, wherein the nickel/gold plating layer is formed with a thickness of below 1μm.

6. The method of claim 1, wherein the laminated body is formed such that openings of each of the plurality of pattern formed plates are formed larger than the opening of the pattern formed plate below it.

7. The method of claim 1, wherein the through hole is filled with a conductive paste or a resin material.

8. The method of claim 1, wherein the second coating layer is made of a nickel/gold plating layer.

9. A method for fabricating a semiconductor package, comprising:

forming a plated copper pattern formed plate by:

forming a first plated copper layer on upper and lower surfaces of a first insulation substrate;

forming a pattern on first plated copper formed at the upper and lower surfaces of the first insulation substrate; and

forming an opening by removing a central portion of the first insulation substrate with the first plated copper pattern formed thereon;

forming an inner circuit pattern formed plate by:

forming a second plated copper pattern on an upper surface or a lower surface of a second insulation substrate;

forming a third plated copper layer on a second plated copper; and

forming an opening by removing a central portion of the second insulation substrate with the second plated copper pattern and the third plated copper formed thereon;

forming a lower circuit pattern formed by:

forming a fourth plated copper pattern on an upper surface or a lower surface of a third insulation substrate;

forming a fifth plated copper layer on the fourth plated copper;

forming an opening by removing a central portion of the third insulation substrate with the fourth plated copper pattern and the fifth plated copper formed thereon;

forming a bonding pad by forming a first nickel/gold plating layer around the opening of the inner circuit pattern formed plate and the lower circuit pattern formed plate;

forming a laminated body by laminating the plated copper pattern formed plate onto the inner circuit pattern formed plate and the inner circuit pattern formed plate onto the lower circuit pattern formed plate using bonding sheets and sequentially attaching the formed plates;

forming a through bore in the laminated body;

forming a sixth plated copper layer on an inner circumferential surface of the through bore, the surface of the laminated body and the first nickel/gold plating layer;

removing the sixth plated copper layer formed on the first nickel/gold plating layer of the laminated body;

forming an outer circuit pattern by patterning a plated copper formed with the sixth plated copper layer formed thereon; and

forming a second nickel/gold plating layer on the first nickel/gold plating layer of the laminated body and at a predetermined portion of the outer circuit pattern formed at an upper surface of the laminated body to form a bonding pad and a ball pad, respectively.

10. The method of claim 9, wherein the insulation substrate is formed of one of glass epoxy, glass polyimide and a bismaleimide triazine resin.

11. The method of claim 9, wherein the first nickel/gold plating layer is formed by an electroless nickel/gold plating, wherein a nickel plating layer is formed, and a gold plating layer is formed at an upper surface of the nickel plating layer.

12. The method of claim 11, wherein the nickel plating layer is formed with a thickness of less than about 0.7μm and the gold plating layer is formed with a thickness of below about 0.3μm, wherein the first nickel/gold plating layer has a thickness of below about 1μm.

13. The method of claim 9, wherein the openings of the plated copper pattern formed plates are larger than the openings of the inner circuit pattern formed plates and the openings of the inner circuit pattern formed plates are larger that the openings of the circuit pattern formed plates.

14. The method of claim 9, wherein the bonding sheets are formed of prepreg sheets, which are formed by setting glass fibers in an adhesive.

15. The method of claim 9, wherein the through hole is filled with a filler comprising a conductive paste or a resin material.

16. The method of claim 9, further comprising:

attaching a solder ball to the ball pad formed at the upper surface of the laminated body, and attaching a heat sink to a lower surface of the laminated body.

17. A method for fabricating a semiconductor package, comprising:

forming a plurality of circuit patterns;

forming a cavity in a central portion of each of the plurality of circuit patterns;

mounting a semiconductor chip within the cavity; and

forming a bonding pad circuit pattern to be connected to the semiconductor within the cavity, wherein a first coating layer is formed with a non-copper metal material at the bonding pad circuit pattern and a copper plating is formed on the first coating layer.

18. The method of claim 17, wherein the copper plating formed on the first coating layer is removed, and a second coating layer is additionally formed with the same metal material as the first coating layer.

19. A method for fabricating a semiconductor package, comprising:

forming a plurality of patterns formed plates, wherein each pattern formed plate is formed by:

forming first plated copper layers on upper and lower surfaces of an insulation substrate;

forming a pattern in the first plated copper layers formed at upper and lower surfaces of the insulation substrate; and

forming an opening by removing a central portion of the insulation substrate with the first plated copper pattern formed thereon;

forming a bonding pad pattern around the opening of at least one of the pattern formed plates;

forming a first coating layer with a non-copper metal material on the bonding pad pattern;

forming a laminated body by laminating the plurality of pattern formed plates to one another, wherein the openings of the plurality of patterns formed plates are aligned to form a cavity;

forming a through bore through the laminated body;

forming a second plated copper layer on the through bore and the first coating layer;

removing the second plated copper layer formed on the first coating layer;

forming a second coating layer with a non-copper metal material on the first coating layer, thereby forming a bonding pad;

mounting a semiconductor chip in the cavity;

connecting the semiconductor chip and the bonding pad by a connection line; and

filling the cavity with a filler.

20. A method of forming a semiconductor package, comprising:

forming a plurality of plates, wherein each plate is formed by:

coating a first coating on a substrate; and

forming an opening in a central portion of the substrate with the first coating thereon;

forming a bonding pad pattern on at least one of the plurality of plates, wherein a second coating is coated onto the bonding pad pattern;

forming a body by stacking the plurality of plates;

forming a through bore in the body; and

coating the through bore with a third coating.

21. The method of claim 20, wherein the second coating comprises a non-copper metal coating and is applied to the bonding pad pattern, wherein the bonding pad pattern is formed around the opening on at least a vertical surface of the opening of at least one of the plurality of plates.

22. The method of claim 21, wherein the second coating comprises Ni-Au.

23. The method of claim 20, wherein the first and third coatings comprises copper.

24. The method of claim 20, further comprising mounting a semiconductor chip to the body by:

forming a heat sink along a bottom surface of the body;

mounting the semiconductor chip to the heat sink; and

connecting the semiconductor chip to the second coating and the bonding pad.

25. The method of claim 20, wherein the plurality of plates comprise three plates.

26. The method of claim 25, wherein the three plates comprise:

an upper plate;

an inner circuit plate formed on a lower surface of the upper plate; and

a lower circuit pattern plate formed on a lower surface of the inner circuit plate, wherein the opening in the upper plate is larger than the opening in the inner circuit plate and the opening in the inner circuit plate is larger than the opening in the lower circuit plate.

27. The method of claim 20, wherein the forming of the body further comprises inserting laminating sheets between the plurality of plates to bond the plates together and form the body.

28. The method of claim 27, wherein the laminating sheets comprise fibers in an adhesive.

29. The method of claim 26, wherein the bonding pad pattern is formed on at least a vertical surface of the opening of at least one of the plurality of plates.

30. The method of claim 29, wherein the second coating on the bonding pad pattern comprises Ni-Au.

31. The method of claim 26, wherein the first and third coatings comprises copper.

32. The method of claim 20, further comprising:

coating a fourth coating on the second coating, wherein the fourth coating is coated thicker than the second coating, and wherein the second and the fourth coatings comprise Ni-Au coatings.

33. The method of claim 20, wherein the substrate comprises:

glass epoxy;

glass polyimide; or

bismaleimide triazine.

34. A semiconductor package, comprising:

a laminated body, comprising:

a plurality of plates laminated into a body, wherein each plate comprises a substrate, a first coating and an opening;

a bonding pad on at least one of the plurality of plates, wherein the bonding pad comprises a metal layer; and

a through bore in the laminated body with a second coating therein;

a heat sink attached to a lower surface of the laminated body;

a semiconductor chip on an upper surface of the heat sink in the openings of the plurality of plates; and

a connector for connecting the semiconductor chip to the laminated body, wherein the connector is connected to the bonding pad of the laminated body.

35. The semiconductor package as claimed in claim 34, wherein the bonding pad on the at least one of the plurality of plates is located on at least a vertical surface of the opening of the at least one of the plurality of plates.